Amendments to the Specification:

Please delete the last paragraph of page 2, which starts with "Referring now to FIG. 1" and extends to page 3.

Please replace the first paragraph of page 3, which starts with "Referring now to FIG. 1" with the following amended paragraph:

A1

Referring now to FIG. 1, a block diagram of a circuit or system 100 is shown illustrating a context for an embodiment of the present invention. The system 100 generally comprises a host portion (or circuit) 102 and a number of enclosures (or circuits) 104-106 ~~104a-104n (where n is an integer)~~. In one example, host circuit 102 may be implemented as a host controller of the system 100. However, in alternative embodiments, host circuit 102 may be implemented as another appropriate number and/or configuration of controller(s) in order to meet the criteria of a particular implementation. Additionally, host circuit 102 may be required to account for (e.g. ignore) other host circuits (not shown) on a particular loop.

Please replace the second paragraph of page 3, which starts with "Enclosures" with the following amended paragraph:

A2

Enclosures 104-106 ~~104a-104n~~ may each be implemented, in one example, as a drive tray. Enclosure 104 ~~104(a)~~ is shown comprising a number of drives 108-112 ~~106a-106n (where n is an integer)~~. Similarly, enclosure 106 ~~104n~~ is shown comprising a number of drives 114-118 ~~108a-108n (where n is an integer)~~. The number of enclosures 104-106 ~~104a-104n~~, as well as the number of drives 108-112 ~~106a-106n~~ and 114-118 ~~108a-108n~~ in each drive portion may be varied accordingly to meet the design criteria of a particular implementation.

Please replace the final paragraph of page 3, which starts with "The system" and extends to page 4 with the following amended paragraph:

The system 100 may illustrate the subsystem monitor 120 and FC driver 124 implemented in an application environment. A number of arrows 125-129 ~~130a-130n~~ may represent redundant loops between the host controller 102 and enclosures 104-106 ~~104a-104n~~. In one example, the arrows 125-129 ~~130a-130n~~ may represent a loop of the system 100. Additionally, a particular direction of the arrows 125-129 ~~130a-130n~~ may be reversed, changing the direction of the redundant loops and/or system loop 125-129 ~~130a-130n~~. The loops 125-129 ~~130a-130n~~ may illustrate a single redundant loop of the system 100. However, the loops 125-129 ~~130a-130n~~ may implement other redundant loops (not shown) in order to meet the criteria of a particular implementation. The FC driver 124 generally holds information regarding the loop ~~130a-130n~~ (e.g., loop map, AL_PAs, drives hard address). The subsystem monitor 120 may retain information from SCSI enclosure service (SES) data received from the drive portions 104-106 ~~104a-104n~~ (e.g., how many drives, slot assigned addresses, etc.). Additionally, the system 100 may allow the presumption that the SES reported order and the physical loop order of the drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~ in the trays 104-106 ~~104a-104n~~ are either the same or the exact reverse order.

A3

Please replace the first paragraph of page 4, which starts with "Data obtained" and with the following amended paragraph:

Data obtained from SES queries may indicate a number of drives present in each tray 104-106 ~~104a-104n~~ (e.g., the drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~). Additionally, the SES data may indicate corresponding FC hard addresses. The hard address for each of the slots is generally set via a connector on a mid-plane (not shown) of each tray 104-106 ~~104a-104n~~. Each of the drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~ may have knowledge of the hard address value by reading an appropriate hard address of the mid-plane of a current slot via an I/C port in the drive 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~.

A4

Please replace the second paragraph of page 4, which starts with "A SES processor" and extends to page 5 with the following amended paragraph:

A5

A SES processor (of the trays 104-106 ~~104a-104n~~, not shown) may acquire and/or store information regarding hard address values for each slot (e.g., drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~) of the trays 104-106 ~~104a-104n~~. The SES processor may also return the hard address information to the host controller 102 via a SES query. Additionally, the controller 102 may obtain the hard addresses of the drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~ via a FC extended link service (e.g., Address Discovery (ADISC)). If the controller 102 determines that all of the drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~ on the loop 125-129 ~~130a-130n~~ acquire assigned hard addresses during loop initialization, then controller mapping (to be discussed in connection with FIGS. 2 and 3) from the SES data to the FC drives found on the loop 125-129 ~~13Oa-13On~~ may be trivial. For example, the controller 102 may simply match the hard addresses of the drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~. Drive trays are generally manufactured such that the hard address of each drive slot is unique. Furthermore, some drive trays may have switch settings in order to set the range of hard addresses such that multiple trays may be on the same loop with no address conflicts. However, if two or more trays 104-106 ~~104a-104n~~ on the loop 125-129 ~~130a-130n~~ have the same switch setting, then the corresponding slots may have the same hard address. When the loop ~~130a-130n~~ initializes the first set of drives (e.g., 108-112 ~~106a-106n~~), the system 100 may obtain hard addresses of the drives 108-112 ~~106a-106n~~ and the second and subsequent drives (e.g., 114-118 ~~108a-108n~~, etc.) may be required to obtain "soft addresses" (e.g., addresses different than the hard addresses). The soft addresses may be implemented to prevent conflicting (e.g., duplicate) hard addresses. In such a scenario, the controller 102 may see two or more tray/slot positions with the same particular hard address value (e.g., x) Therefore, two or more drives may have the same hard address x. The system 100 is normally required to correctly match the appropriate trays/drives with allowable addresses.

Please replace the first paragraph of page 5, which starts with "The system" with the following amended paragraph:

The system 100 may implement proper correspondence based on the following data available to the controller 102 (i) SES data from an enclosure services monitor (ESM) that may list the number of drives installed and respective assigned hard addresses; (ii) whether or not a particular drive is bypassed from the loop 125-129 ~~130a-130n~~ (e.g., contained within the SES data); (iii) a loop map that may list current addresses of the trays and/or drives on the loop 125-129 ~~130a-130n~~; and/or (iv) a loop order of the trays and/or drives on the loop 125-129 ~~130a-130n~~. In order for the system 100 to implement the proper correspondence, certain assumptions may be made. By designing the system 100 with the broadest assumptions, multiple drive trays from multiple vendors may be accommodated. Specific knowledge of how a particular drive tray is internally wired may not be required (e.g., a relative position of the ESM to the drive or a particular direction of the loop through the tray). Therefore, the system 100 may have broad applicability. However, in a particular implementation the present invention may leverage specific knowledge from a particular drive tray 104-106 ~~104a-104n~~. An initial condition may be for each ESM to be adjacent to or in the middle of the drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~ in a particular tray 104-106 ~~104a-104n~~ on the loop map.

A6

Please replace the final paragraph of page 5, which starts with "Referring now" and extends to page 6 with the following amended paragraph:

Referring now to FIG. 2, an embodiment of a storage system 200 of the present invention is shown. Storage system 200 may include a controller 210, such as a bridge controller, and at least one enclosure 104-106 ~~104a-104n~~. Controller 210 ~~110~~ may include components and circuitry of host circuit 102 as shown in FIG. 1. Integrated within each enclosure 104-106 ~~110~~ may be an enclosure services module 130-132 ~~130~~. Enclosure services module 130-132 ~~130a-130n~~ associated with each enclosure 104-106 ~~104a-104n~~ respectively may provide information to controller 210 ~~110~~ such as the number of drives installed and their respective hard addresses. Enclosure services

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A7

module may include "in" and "out" ports from which other enclosures 104-106 ~~104(a)-104(n)~~ and controller 210 may be interconnected.

Please replace the first paragraph of page 6, which starts with "Referring now to FIGS. 3A and 3B" with the following amended paragraph:

A8

Referring now to FIGS. 3A and 3B, embodiments of enclosures 300, 310 are shown. Enclosure 300 shown in FIG. 3A ~~FIG. A~~ utilizes internal wiring where the SES device may be in an "in-to-out" path. Enclosure 310 shown in FIG. 3B utilizes internal wiring where the SES device may be in an "out-to-in" path. Both types of wiring may be frequently utilized today in enclosure service modules. Included within each enclosure 300, 310 may be a bypass block, a SES device, and a number of drives. An advantageous aspect of the present invention is the ability to support the associating and mapping of devices with both types of internal wiring.

Please replace the second paragraph of page 6, which starts with "Referring to FIG. 4" with the following amended paragraph:

A9

Referring to FIG. 4, a block diagram of a method (or process) 400 ~~300~~ illustrating an operation of the present invention is shown. The method 400 ~~300~~ may rely on a process of elimination via a repetitive loop. For example, three drive trays 104-107 ~~104a-104n~~ are shown with a corresponding enclosure service module (e.g., ESM1, ESM2, and ESM3). A number of drives of the system 400 ~~300~~ may be numbered Dl through D9. Each of the ESMs may comprise a number of the drives D1-D9. For example, ESM1 may comprise the drives Dl-D3, ESM2 may comprise D4-D6 and ESM3 may comprise the drives D7-D9. However, a particular number of ESMs, as well as drives may be varied in order to meet the criteria of a particular implementation. The hard addresses of each of the drives Dl-D9 maybe labeled Hn, respectively. The drives D1-D9 may have duplicate hard addresses. A current address of each of the drives Dl-D9 maybe labeled Cn. Additionally, each of the ESMs may be implemented with a hard address and current address, respectively. In the case of address conflicts, the current

A4

addresses Cn of the system 200 may be rather random. The current addresses Cn may comprise a loop map obtained from the FC loop initialization processes. Each drive Dl-D9 may be queried to obtain a hard address Hn and current address Cn.

Please replace the final paragraph of page 6, which starts with "A detailed description" and extends to page 7 with the following amended paragraph:

A10

A detailed description of an operation of the system 400 ~~300~~ is described below. If the tray ESM2 is being mapped first, then a match on the hard addresses H1 may occur in both the forward direction (e.g., the drives D4, D5 and D6) and reverse direction (e.g., the drives Dl, D2 and D3). In the ESM2 mapping example, the method 300 may continue until the tray ESM1 may be mapped having only one match. At that point, mapping of the tray ESM2 may allow only one match because the drives Dl, D2 and D3 may be marked as already mapped. Additionally, the hard address H1 of the tray ESM3 may get a double match if mapped first. The method 400 ~~300~~ may be initiated to notice an end of the loop. Therefore, the last ESMn may be required to associate with the last set of drives. However, a designer may have an implementation choice as to whether to merely retry the comparison ratio or implement extra logic in the comparison routine.

Please replace the second paragraph of page 8, which starts with "(D) in the state 508" with the following amended paragraph:

A11

(D) in the state 508 the system 500 may create a corresponding loop map that may utilize the hard addresses of the loop devices (e.g., ESM and drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~). A particular hard address may be obtained via address discovery (FC extended link service);

Please replace the third paragraph of page 8, which starts with "(E) in the states 510" with the following amended paragraph:

A12

(E) in the states 510, 512 and 514 the system 500 may find the position of the

ESM that may supply the SES data on the loop map and use the loop map position as an anchor to compare the hard addresses in the SES data to the hard addresses in the loop map. The comparison may be required to be done in the forward and reverse direction (e.g., cannot assume a direction of the loop) and may account for the possibility that the ESM anchor may be at the beginning, the end, or in the middle of the group of drives for each set of SES data describing a group of drives in the tray until all the drives have been mapped. Additionally, the loop may have to be repeated several times in order to map all the drives of the various loop devices. However, when performing the compare (e.g., the compare state 514) of the SES slot ID data to the hard address version of the loop map, the system 500 may be required to logically ~~tologically~~ remove the ESM device loop map. For example, if the ESM location is in a predetermined portion (e.g., a middle position) of the drives, the ESM location may corrupt the compare. The compare may be corrupted, since the ESM location is generally not accounted for in the SES drive list data; and

A12

Please replace the fourth paragraph of page 8, which starts with "(F) in the states 516" with the following amended paragraph:

(F) in the states 516, 518, 520, 521 and 522 the system 500 may if only one match is found, mark the drives 108-112 ~~106a-106n~~ and/or 114-118 ~~108a-108n~~ as mapped and continue or if more than one match is found, mark the comparison as ambiguous and repeat the mapping stages 512-522.

Please replace the final paragraph of page 8, which starts with "Conventional Methods" and extends to page 9 with the following amended paragraph:

A13

Conventional methods for mapping drives with soft addresses to physical tray/slot positions utilize a position of the ESM device in the loop map as a delimiter for the drive trays. However, the system 100 (200, 400, or 500) may not assume a particular layout inside the device portions 104-107 ~~104a-104n~~ (e.g., is the ESM in the middle, before, or after the drives) or the loop direction within the drive portion 104-107 ~~104a-~~

#13

~~104n~~. The system 100 (200, 400, or 500) may not rely on the position of the ESM device in the loop map.

Please replace the first paragraph of page 9, which starts with "Since the system" and extends to page 10 with the following amended paragraph:

#14

Since the system 100 (200, 400, or 500) may not assume a particular layout, an improvement may be achieved by implementation of state 521 ~~421~~. In the mapping of enclosures where the internal wiring is of a type as shown in FIG. 3B, an error in the algorithm may appear without implementation of state 521 ~~421~~. An advantage of the present invention may the ability to remove the error. If an enclosure mapping fails, mapping may proceed to the next enclosure and the failed mapping may be retried later in the process. If an enclosure is successfully mapped, it may be effectively removed from the loop data. For example, suppose two enclosures of FIG. 3B were connected as shown in FIG. 2. The loop map may be as follows:

1. D1(enclosure#1)
2. D2(enclosure#1)
3. D3(enclosure#1)
4. D1(enclosure#2)
5. D2(enclosure#2)
6. D3(enclosure#2)
7. SES(enclosure#2)
8. SES(enclosure#1)
9. Bridge Controller

However, mapping of enclosure #1 may fail because the SES device of enclosure 1 may not be adjacent to its drives. Mapping of enclosure #2 may succeed. Upon successful mapping, the SES device and drives of enclosure #2 may be removed from loop data used for further mapping per state 521 ~~421~~. Therefore, the following loop map may include:

1. D1(enclosure#1)
2. D2(enclosure#1)

#4

3. D3(enclosure#1)
4. SES(enclosure#1)
5. Bridge Controller

Upon a retry of the mapping of enclosure #1 may succeed because the SES device of enclosure #1 may be adjacent to its drives.